UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/829,495 | 04/22/2004 | William Taylor | 20103/030290 | 6926 |

83417 7590 10/01/2009

AT&T Legal Department - HFZ
ATTN. Patent Docketing
One AT&T Way
Room 2A-207
Bedminstor, NJ 07921

| EXAMINER | |
|---|---|
| SHIVERS, ASHLEY L | |
| **ART UNIT** | **PAPER NUMBER** |
| 2419 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 10/01/2009 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/829,495 | TAYLOR ET AL. | |
| | Examiner | Art Unit | |
| | ASHLEY L. SHIVERS | 2419 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *July 23, 2009 (RCE)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Art Unit: 2419

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 23, 2009 has been entered.

### *Response to Amendment*

2. Applicant's amendment filed on July 23, 2009 has been entered. Claims 1-21 have been amended. Claim 22 is canceled. Claim 23 has been added. Claims 1-21 and 23 are still pending in this application, with claims 1 and 13 being independent.

### *Claim Objections*

3. Claim 1 is objected to because of the following informalities:

--In claim 1, replace –monitor switches in a first logical circuit—with --monitor switches of a first logical circuit--.

Appropriate correction is required.

## *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over McAllister et al. (**U.S. Patent No. 6,697,329**), hereinafter referred to as McAllister in view of Ashton et al. (**U.S. Patent No. 6,181,679**), hereinafter referred to as Ashton in further view of Heeren et al. (**U.S. Patent No. 6,311,288**), hereinafter referred to as Heeren.

Regarding claim 1, McAllister teaches a method for fail-safe renaming of logical circuit identifiers for rerouted logical circuits in a data network, the method comprising:

providing a network management module (**NMS; See Fig. 2A, #46**) in communication with first and second local access and transport areas (**Nodes 32A and 32D are interpreted as the nodes of the LATAs as 32A is located in Montreal and 32D is located in Toronto; See Fig. 1, #28a, #28d and Fig. 2A, #32a and #32d**) and a failover network (**Nodes 32B and 32C, 32E and 32F are interpreted as the nodes of the failover networks**), the first local access and transport area in communication with the second local access and transport area via an inter-exchange carrier (**Node 32G is interpreted as the node of the IXC; See Fig. 2B, #32G**), the failover network in communication with the first and second local access and transport areas and separate from the inter-exchange carrier (**Using at least one alternate path indication each defining at least one network path element of the connection located between the source network element and the destination network element, each alternate path indication not being identical to the preferred routing indication; See col. 4, lines 62-66**), and the network management module to:

reroute the data via the second logical circuit (**When the primary link fails the source re-routes the connection along the nodes and links in its alternate path; See col. 11, lines 34-36**), wherein

the first logical circuit connects the first and second local access and transport areas via the inter-exchange carrier (**Node 32G is interpreted as the node of the IXC; See Fig. 2B, #32G**), the switches located in the first and second local access and transport areas (**Nodes 32A and 32D are interpreted as the switches in the first and second LATAs; See Fig. 2A, #32A and #32D**);

the second logical circuit connects the first and second local access and transport areas via the failover network (**Alternate links going through Nodes 32B, C, E and F; See Fig. 2A**).

McAllister fails to teach of the network management module monitoring the switches of a first logical circuit, renaming a first logical circuit identifier for the first logical circuit to a second logical circuit identifier for a second logical circuit utilized for rerouting data from the first logical circuit, receiving status information indicating that one of the switches is discarding frames or cells and identifying, in response to the status information, a failure in the first logical circuit.

Ashton teaches of the network management system that:

monitors switches in a first logical circuit (**The network management system receives status and configuration data from the nodes. The automation table detects the faults or failure in a virtual circuit segment and responds automatically to such faults or failures by either taking action directly to alter the configuration of the network; See col. 3, lines 44-51**);

receives status information indicating that one of the switches is discarding frames or cells (**The network management system receives status and configuration data from the nodes. The automation table detects the faults or failure in a virtual circuit segment and responds automatically to such faults or failures by either taking action directly to alter the configuration of the network; See col. 3, lines 44-51**); and

identifies in response to the status information, a failure in the first logical circuit (**See col. 3, lines 44-51**).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method of McAllister to include monitoring the switches in a first logical circuit, receiving status information indicating that one of the switches is discarding frames or cells and identifying, in response to the status information, a failure in the first logical circuit taught by Ashton in order to determine when the packets need to be re-routed to prevent further packet loss or delay in packet processing.

McAllister in view of Ashton still fails to teach of renaming the first logical circuit identifier to the second logical circuit identifier.

Heeren teaches of renaming a first logical circuit identifier for the first logical circuit to a second logical circuit identifier for a second logical circuit utilized for rerouting data from the first logical circuit (**If the primary destination (Port 2 DLCI 54) is unavailable the frames are switched to Port 3 DLCI 54, wherein the identifier names are the same and interpreted as the first identifier being renamed to the second; See col. 10, lines 23-25**).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method of McAllister in view of Ashton to include renaming the first logical circuit identifier to the second logical circuit identifier taught by Heeren in order to make a transparent transition from one logical circuit to the other without the customer knowing that the circuit has failed.

Regarding claim 2, McAllister further teaches the method of claim 1, wherein the network management module renames the first logical circuit identifier for the first logical circuit to the second logical circuit identifier for the second logical circuit utilized for rerouting data from the first logical circuit, by:

provisioning the second logical circuit in the network device for rerouting the data from the first logical circuit, wherein provisioning the second logical circuit includes assigning the second logical circuit identifier to identify the second logical circuit (**The operator could specify an alternate route for connection as node 32A, node 32E, node 32F and node 32D or node 32A, node 32b, node 32C and node 32D. The operator uses the NMS to select or confirm the appropriate node and link identifiers for these paths; See col. 7, lines 41-49**).

McAllister fails to teach of accessing a network device provisioned for routing data over the first logical circuit, deleting the first logical circuit in the network device upon detecting a failure in the first logical circuit and renaming the first logical circuit identifier to the second logical circuit identifier.

Ashton teaches of:

accessing a network device provisioned for routing data over the first logical circuit (**The intersegment connections can be checked by the network management system to determine if the virtual circuit is complete and correct, and to permit rapid and accurate establishment of alternate route virtual circuit connections between nodes in the face of failures in the virtual circuit segments. The network management system receives status and configuration data from the nodes; See col. 3, lines 36-48**); and

deleting the first logical circuit in the network device upon detecting a failure in the first logical circuit (**The "F" bit is used by a network management system to remove the failed segments from service and to permit the substitution of a segment which is operative; See col. 3 lines 22-24**).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method of McAllister to include accessing a network device provisioned for routing data over the first logical circuit and deleting the first logical circuit in the network device upon detecting a failure in the first logical circuit taught by Ashton in order to remove bad links from the connection so that further packet loss does not occur.

McAllister in view of Ashton still fails to teach of renaming the first logical circuit identifier to the second logical circuit identifier.

Heeren teaches of renaming a first logical circuit identifier for the first logical circuit to a second logical circuit identifier (**If the primary destination (Port 2 DLCI 54) is unavailable the frames are switched to Port 3 DLCI 54, wherein the identifier names are the same and interpreted as the first identifier being renamed to the second; See col. 10, lines 23-25**).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method of McAllister in view of Ashton to include renaming the first logical circuit identifier to the second logical circuit identifier taught by Heeren in order to make a transparent transition from one logical circuit.

Regarding claim 3, McAllister further teaches the method of claim 1, wherein the second logical circuit is a logical failover circuit (**When the primary link fails the source re-routes the connection along the nodes and links in its alternate path; See col. 11, lines 34-36**).

Regarding claim 4, McAllister further teaches the method of claim 1, wherein the second logical circuit is a currently unused logical circuit (**When the primary link fails the source re-routes the connection along the nodes and links in its alternate path; See col. 11, lines 34-36**).

Regarding claim 5, McAllister teaches the method of claim 1, but fails to teach of the first logical circuit identifier being a data link connection identifier (DLCI).

Ashton teaches of the first logical circuit identifier being data link connection identifiers (DLCI) (**The virtual circuit segments are identified by a DLCI; See col. 3 lines 16-18**).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method of McAllister to include the second logical circuit identifier being a data link connection identifier taught by Ashton in order to tell the network how to route the data.

Regarding claim 6, McAllister teaches the method of claim 1, but fails to teach of the second logical circuit identifier being a data link connection identifier (DLCI).

Ashton teaches of the second logical circuit identifier being data link connection identifiers (DLCI) (**The virtual circuit segments are identified by a DLCI; See col. 3 lines 16-18**).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method of McAllister to include the first logical circuit identifier being a data link connection identifier taught by Ashton in order to tell the network how to route the data.

Regarding claim 7, McAllister further teaches the method of claim 1, wherein the first logical circuit identifier is a virtual path/virtual circuit identifier (VPI/VCI) (**See Fig. 5**).

Regarding claim 8, McAllister further teaches the method of claim 1, wherein the second logical circuit identifier is a virtual path/virtual circuit identifier (VPI/VCI) (**See Fig. 5**).

Regarding claim 9, McAllister further teaches the method of claim 1, wherein the first and second logical circuits are permanent virtual circuits (**See col. 3, lines 28-32**).

Regarding claim 10, McAllister further teaches the method of claim 1, wherein the first and second logical circuits are switched virtual circuits (**See col. 3, lines 28-32**).

Regarding claim 11, McAllister teaches the method of claim 1, but fails to teach of the network being frame relay.

Ashton teaches of the data network being a frame relay network (**Fig. 1 is shown as a frame relay network; See col. 4 lines 55-57**).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method of McAllister to include the data network being a frame relay network taught by Ashton in order to emphasize the type of network that can be implemented.

Regarding claim 12, McAllister further teaches the method of claim 1, wherein the first logical circuit is established in an asynchronous transfer mode (ATM) network (**See col. 6, lines 7-8**).

Regarding claim 13, McAllister teaches a system for fail-safe renaming of logical circuit identifiers for rerouted logical circuits in a data network, the system comprising:

a network device (**Nodes 32A and 32D; See Fig. 2A**) to establish a communication path for a logical circuit and a logical failover circuit, the logical circuit connecting first and second local access and transport areas (**Nodes 32A and 32D are interpreted as the nodes of the LATAs as 32A is located in Montreal and 32D is located in Toronto; See Fig. 1, #28a, #28d and Fig. 2A, #32a and #32d**) via an inter-exchange carrier (**Node 32G is interpreted as the node of the IXC; See Fig. 2B, #32G**), and the logical failover circuit connecting the first and second local access and transport areas via a failover network (**Nodes 32B and 32C, 32E and 32F are interpreted as the nodes of the failover networks**) that is separate from the inter-exchange carrier (**Using at least one alternate path indication each defining at least one network path element of the connection located between the source network element and the destination network element, each alternate path indication not being identical to the preferred routing indication; See col. 4, lines 62-66**);

a logical element module in communication with the network device to configure the logical circuit and the logical failover circuit (**The user interface means provided by the NMS facilitates the input of the ODR SPVC, including the preferred or primary path and the alternate path; See col. 7, lines 49-52**); and

a network management module (**NMS; See Fig. 2A, #46**) in communication with the first and second local access and transport areas (**Nodes 32A and 32D are interpreted as the nodes of the LATAs as 32A is located in Montreal and 32D is located in Toronto; See Fig. 1, #28a, #28d and Fig. 2A, #32a and #32d**) and the failover network (**Nodes 32B and 32C, 32E and 32F are interpreted as the nodes of the failover networks**) to:

establish the communication path for the logical failover circuit through the failover network to reroute data from the failed logical circuit (**Alternate links going through Nodes 32B,C,E and F; See Fig. 2A**); and

assign a logical failover circuit identifier to identify the logical failover circuit (**The operator could specify an alternate route for connection as node 32A, node 32E, node 32F and node 32D or node 32A, node 32b, node 32C and node 32D. The operator uses the NMS to select or confirm the appropriate node and link identifiers for these paths; See col. 7, lines 41-49**), wherein

the switches of the logical circuit are located in the first and second local access and transport areas (**Nodes 32A and 32D are interpreted as the switches in the first and second LATAs; See Fig. 2A, #32A and #32D**).

McAllister fails to teach of monitoring the switches of the logical circuit, receiving status information indicating that one of the switches is discarding frames or cells, identifying, in response to the status information, a failure in the logical circuit, deleting the communication path for the failed logical circuit in the network device and renaming a logical circuit identifier for the failed logical circuit to a logical failover circuit identifier.

Ashton teaches of:

monitoring switches in a logical circuit (**The network management system receives status and configuration data from the nodes. The automation table detects the faults or failure in a virtual circuit segment and responds automatically to such faults or failures by either taking action directly to alter the configuration of the network; See col. 3, lines 44-51**);

receiving status information indicating that one of the switches is discarding frames or cells (**The network management system receives status and configuration data from the nodes. The automation table detects the faults or failure in a virtual circuit segment and responds automatically to such faults or failures by either taking action directly to alter the configuration of the network; See col. 3, lines 44-51**);

identifying, in response to the status information, a failure in the logical circuit (**See col. 3, lines 44-51**); and

deleting the communication path for the failed logical circuit in the network device (**The "F" bit is used by a network management system to remove the failed segments from service and to permit the substitution of a segment which is operative; See col. 3 lines 22-24**).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the system of McAllister to include monitoring the switches in a logical circuit, receiving status information indicating that one of the switches is discarding frames or cells, identifying, in response to the status information, a failure in the logical circuit and deleting the communication path for the failed logical circuit in the network device taught by Ashton in order to determine when the packets need to be re-routed to prevent further packet loss or delay in packet processing.

McAllister in view of Ashton still fails to teach of renaming the first logical circuit identifier to the second logical circuit identifier.

Heeren teaches of renaming a first logical circuit identifier for the first logical circuit to a second logical circuit identifier for a second logical circuit utilized for rerouting data from the first logical circuit (**If the primary destination (Port 2 DLCI 54) is unavailable the frames are switched to Port 3 DLCI 54, wherein the identifier names are the same and interpreted as the first identifier being renamed to the second; See col. 10, lines 23-25**).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the system of McAllister in view of Ashton to include renaming the first logical circuit identifier to the second logical circuit identifier taught by Heeren in order to make a transparent transition from one logical circuit to the other without the customer knowing that the circuit has failed.

Regarding claim 14, McAllister teaches of the system of claim 13, but fails to teach of wherein the logical circuit identifier being a DLCI.

Ashton teaches of the logical circuit identifier being data link connection identifiers (DLCI) (**The virtual circuit segments are identified by a DLCI; See col. 3 lines 16-18**).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the system of McAllister to include the logical circuit identifier being a data link connection identifier taught by Ashton in order to tell the network how to route the data.

Regarding claim 15, McAllister teaches of the system of claim 13, but fails to teach of the logical failover circuit identifier being a DLCI.

Ashton teaches of the logical failover circuit identifier being a data link connection identifier (DLCI) (**The virtual circuit segments are identified by a DLCI; See col. 3 lines 16-18**).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the system of McAllister to include the and logical failover circuit identifier being a data link connection identifier taught by Ashton in order to tell the network how to route the data.

Regarding claim 16, McAllister further teaches the system of claim 13, wherein the logical circuit identifier is a virtual path/virtual circuit identifier (VPI/VCI) (**See Fig. 5**).

Regarding claim 17, McAllister further teaches the system of claim 13, wherein the logical failover circuit identifier is a virtual path/virtual circuit identifier (VPI/VCI) (**See Fig. 5**).

Regarding claim 18, McAllister further teaches the system of claim 13, wherein the logical circuit and the logical failover circuit are permanent virtual circuits (**See col. 3, lines 28-32**).

Regarding claim 19, McAllister further teaches the system of claim 13, wherein the logical circuit and the logical failover circuit are switched virtual circuits (**See col. 3, lines 28-32**).

Regarding claim 20, McAllister teaches the system of claim 13, but fails to teach of the network being frame relay.

Ashton teaches of the data network being a frame relay network (**Fig. 1 is shown as a frame relay network; See col. 4 lines 55-57**).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the system of McAllister to include the data network being a frame relay network taught by Ashton in order to emphasize the type of network that can be implemented.

Regarding claim 21, McAllister further teaches the system of claim 13, wherein the logical circuit is established in an asynchronous transfer mode (ATM) network (**See col. 6, lines 7-8**).

Regarding claim 23, McAllister further teaches the method of claim 1, wherein the switches communicate the data via the first logical circuit (**An SPVC call setup message; See col. 5, lines 10-11**), and wherein the network management module is separate from the switches that communicate the data (**NMS; See Fig. 2A, #46**).

### *Response to Arguments*

6. Applicant's arguments with respect to claims 1-21 and 23 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

7. Any response to this action should be **faxed** to (571) 273-8300 or **mailed** to:

Commissioner of Patents,
P.O. Box 1450
Alexandria, VA 22313-1450

**Hand delivered responses should be brought to:**
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ASHLEY L. SHIVERS whose telephone number is (571) 270-3523. The examiner can normally be reached on Monday-Friday 8:30-5:00 EST.

Art Unit: 2419

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chirag Shah can be reached on (571) 272-3144. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. L. S./
Examiner, Art Unit 2419
9/29/2009
/Chirag G Shah/
Supervisory Patent Examiner, Art Unit 2419